Evaluation Board for Low Cost, Low Power, CMOS Gerneral Purpose Dual Analog Front End

EVAL-AD73322EB

FEATURES

Up to 4 CODECS (2 Devices)Can Be Configured In Cascade.

Interfaces To The ADSP-2181 EZ-KIT LITE.

Stand Alone Capabiliy.

Daughter Board for Quick Demo of CODECS

Various Link Options For Setting Configuration.

On Board +5V Regulator.

On Board Clock Generator.

On Board Anti-Aliasing.

EVAL-AD73322EZ / EVAL-AD73322EB

The AD73322 Evaluation board can be supplied either with or without an ADSP2181 EZ-KIT LITE Board. **EVAL-AD73322EZ** contains an AD73322 evaluation board and a modified EZ-KIT LITE board. **EVAL-AD73322EB** contains an AD73322 evaluation board and the material needed to modify a customers existing EZ-KIT LITE board.

An existing EZ-KIT LITE board can easily be modified to interface with the EVAL-AD73322EB board by carrying out the following modification:

- Solder the 40 pin right angle header (included in the EVAL-AD73322EB package) onto the EZ-KIT LITE board in position P3, pins 11-50, with the header pins facing the edge of the board.

INTRODUCTION

The AD73322 is a dual front-end processor for general purpose applications including speech and telephony. It features two 16-bit A/D conversion channel and two 16-bit D/A conversion channel. Each channel provides 70 dB signal-to-noise ratio over a voiceband signal bandwidth.

The AD73322 is suitable for a variety of applications in the speech and telephony area including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multichannel active control applications.

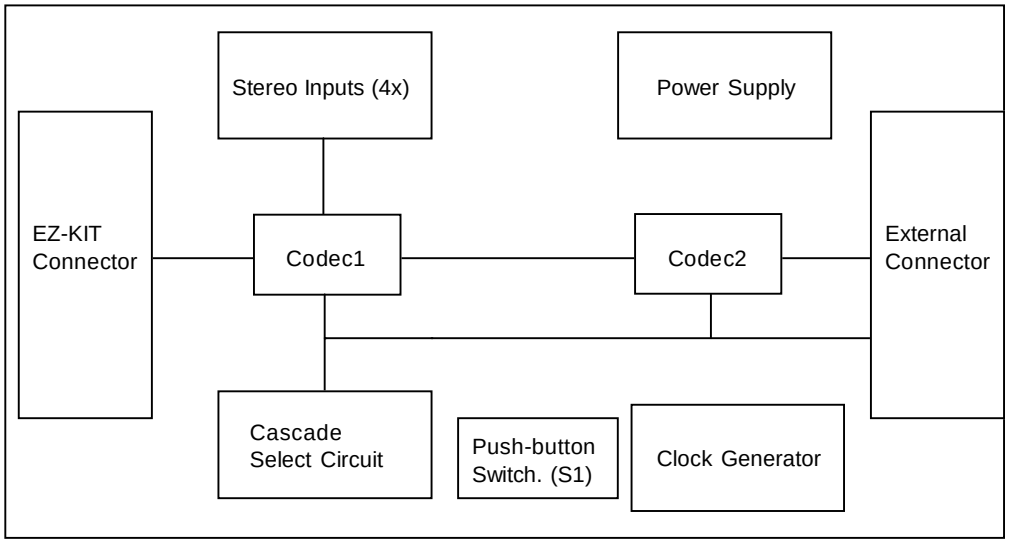
The gains of the A/D and D/A conversion channels are programmable over 38dB and 21dB ranges respectively. An on-chip reference voltage is included to allow single supply operation. A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines.

The AD73322 is available in both 28-lead SOIC and 44-lead LQFP packages.

Full data on the AD73322 is available in the AD73322 data sheet available from Analog Devices and should be consulted in conjunction with this Technical Note when using the Evaluation Board.

Included on the evaluation board, along with the two AD73322 Codecs are a power supply circuit, a clock generator circuit, a cascade selector circuit and a daughter board. These are explained in detail on the next page.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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Power Supply Circuit.

D.C. power between 8V & 12V is applied to the board through either connector J9 or J10 (positive is on the outer sleeve). These connectors are connected together in a loop through arrangement which is intended for supplying the external voltage to the EZ-KIT LITE which accompanies this evaluation board. The power supply shipped with the EZ-KIT Lite is suitable for powering both the AD73322 board and the EZ-KIT LITE board. Diode, D1, prevents damage due to accidental reversal of the supply. Regulator, U5, generates the +5V necessary for all the analog and digital circuitry on the board.

Clock Generator Circuit.

The oscillator, U8, provides two stable crystal controlled outputs of 16.384MHz or 8.192MHz. One of these frequencies is selected by LK4 to produce the on-board generated clock signal. LK5 is used to select this clock signal or the EZ-KIT LITE clock signal as the master clock (MCLK). MCLK is used as the main clock for the AD73322 and is also used for the external synchronisation circuit for the SE and $\overline{\text{RESET}}$ signals. The board is shipped with 16.384MHz selected as the default clock frequency.

Cascade Selector circuit.

This is programmed by software to determine the number of codecs in cascade. The 74HC253(U3) is a 2 channel 4-1 multiplexer which is automatically controlled by software to select which codec has its SDO and SDOFS returned to the DSP. The process of downloading a user program automatically sets the multiplexer to the required setting. If the user develops their own sample programs, then it is necessary to select the correct multiplexer settings for the cascade configuration. See Table 1 for details of required multiplexer settings for various cascade settings.

Daughter Board.

The daughter board is used to provide easy configuration for using the demonstation programs provided with the evaluation board. It provides circuitry for a stereo line input at stereo jack J13. These inputs are single-ended but are put through a pair of single-ended to differential converters to provide two fully differential inputs at the two input channels of device U1. The analog outputs of U1 are connected in a single-ended mode through an ac-coupling RC filter to provide an output which can drive either the inputs of computer speakers or walkman headsets.

It is possible for the user to configure their own input circuitry on a similar daughter board. The daughter board dimensions are detailed in Figure 9 .

OPERATING THE AD73322 EVALUATION BOARD

The AD73322 EVAL BOARD is designed to be interfaced directly to the EZ-KIT LITE which is an entry level demonstration tool for the ADSP-2181 DSP. The interface to the EZ-KIT LITE is provided through the connector J11. Alternatively, the board may be connected to the Texas Instrument TMS320C5XX EVM via connector J12.

Before applying power and signals to the evaluation board it is essential to ensure that all links are set as required for the desired operating mode. The function of all links is explained below.

Link	Board	Function
LK1	Main Board	Connects TFS to RFS on DSP.
LK2	Main Board	Connects SE to VDD or FL0 of DSP.
LK3	Main Board	Connects $\overline{\text{RESET}}$ to FL2 or $\overline{\text{FL2}}$ of DSP.
LK4	Main Board	Selects between the 16.384MHz or 8.192MHz outputs from the on-board clock circuit.
LK5	Main Board	Selects the on-board generated clock or DSP clock as the master clock for the board.

Boards are shipped with the following link settings.

LINK NO.	POSITION	FUNCTION
LK1	1 to 2	TFS tied to RFS.
LK2	1 to 2	SE tied to FL0 of DSP.
LK3	1 to 2	RESET tied to FL2 of DSP.
LK4	1 to 2	16.384MHz selected as the output of the crystal oscillator.
LK5	2 to 3	CLK tied to on board crystal oscillator.

INTERFACING TO THE EZ-KIT LITE

The EZ-KIT LITE board must be modified by the inclusion of a right-angled male header strip (20 x 2) in positions 11 to 50 of connector P3. This header mates to a matching female connector (J11) on the AD73322 Evaluation board.

- Connect the AD73322 EVAL BOARD to the EZ-KIT LITE BOARD using J11.
- Plug the daughter board onto the EVAL BOARD using J1, J2, J5 and J6.
- Connect the serial cable between PC and EZ-KIT LITE.
- Attach the power loop through cable between J10 of the EVAL BOARD and the power input of the EZ-KIT BOARD.
- Apply power to the setup via J9 using the DC PSU supplied with the eval board.

When power is applied the green LED on EZ-KIT BOARD should remain lit while red LED should flash to indicate system is ready to accept a program. If any difficulty is experienced please refer to the EZ-KIT LITE REFERENCE MANUAL.

Analog I/O.

The analog I/O to each codec is designed to be flexible and the evaluation board provides some prototyping space for user supplied input/output circuitry. Codecs 1(U1) uses a pair of stereo (3 pole) 3.5 mm miniature jack plugs (J13 through J16) to connect signals to/from the evaluation board via single-in-line sockets J12 and J2 and from the prototyping space through J5 and J6. Codecs 2(U2) uses single-in-line sockets J3 and J4 and from the prototyping area through J7 and J8.

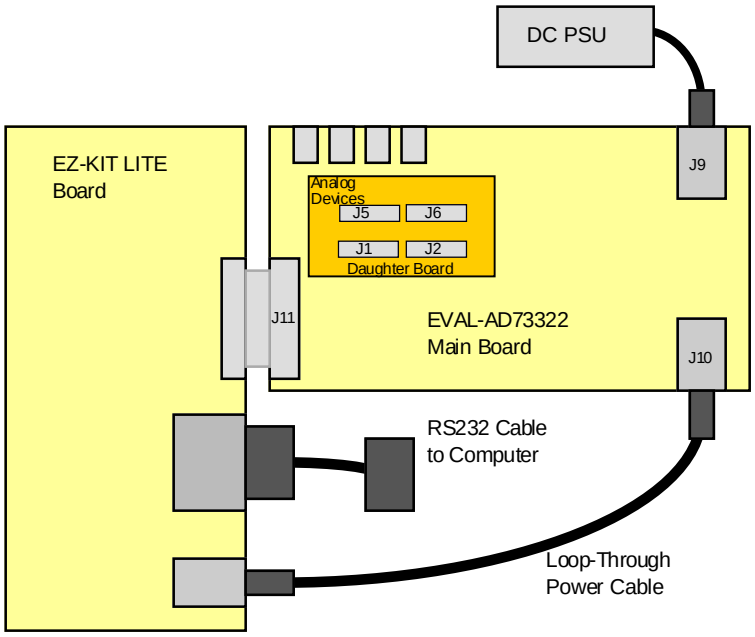

Fig. 1: Interfacing to the EZ-KIT LITE.

LOADING DEMO PROGRAMS.
Follow EZ-KIT instructions for installation of EZ-KIT software. Activate the windows FILE MANAGER and create a directory for the AD73322 diskette (example C:\ADI_DSP\EZ-73322) Copy the contents of the AD73322 demo programs diskette into this directory. Alternatively the demo programs can be run from the diskette drive. Close down FILE MANAGER.

The AD73322 evaluation board uses the user program facility of the EZ-KIT LITE PC based software to download its demonstration programs. Therefore it does not have a menu of demonstration options but instead the various demonstrations must be downloaded as one would download a user program under the existing EZ-KIT LITE software. Please refer to the EZ-KIT LITE reference manual for more details of this feature (page 6-13).

Activate the EZ-KIT LITE -Monitor host program and select the LOADING option. The red LED on the EZ-KIT LITE board must be flashing while doing this operation. Use the RESET button on the EZ-KIT board to make the LED flash if necessary.

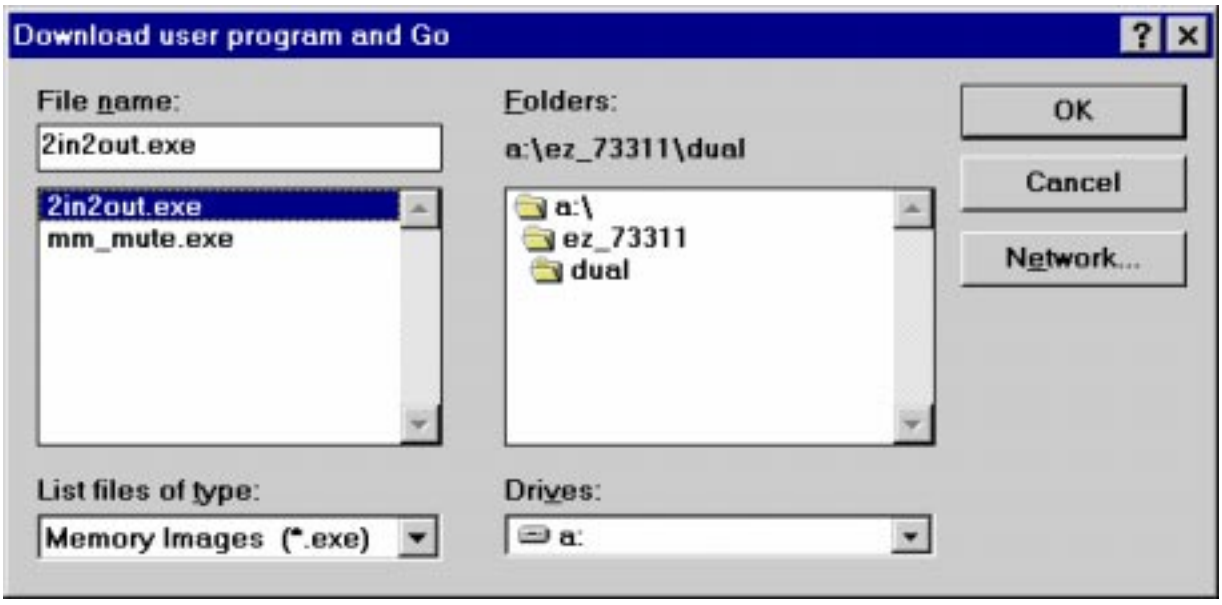

Fig. 2: Download User Program and Go menu

From this select the DOWNLOAD USER PROGRAM AND GO menu. This opens the window shown in Fig. 2.

AD73322 SINGLE CODEC DEMO PROGRAMS
These demo programs use a single channel on an AD73322 device. The other channel is powered-down except for the SPORT section which must remain active to support cascading operation.

Loop-Through (64 kHz) (a:\EZ_73322\single\1in1out.exe)
In this demo a single AD73322 codec is configured for loop-through operation with input samples being passed through to the output at a 64 kHz rate. This sampling rate gives low group delay sampling which is suitable for active control applications.

File(s) used are: \EZ_73322\single\1in1out.dsp

Build using: \EZ_73322\single\make.bat

Loop-Through (8 kHz) (a:\EZ_73322\single\1inout8k.exe)
This demo is similar to the 64 kHz sampling demo except that the sampling rate is reducedto 8 kHz.

File(s) used are: \EZ_73322\single\1inout8k.dsp

Build using: \EZ_73322\single\make.bat

Tone Generator (a:\EZ_73322\single\sine_gen.exe)
This demo generates a 1 kHz tone by updating a function generation algorithm at an 8 kHz rate. The AD73322 channel is set for a sample rate of 8 kHz which is uses to determine the function generation update points.

File(s) used are: \EZ_73322\single\init_cod.dsp \EZ_73322\single\sin.dsp \EZ_73322\single\sine_gen.dsp

Build using: \EZ_73322\single\up.bat

DTMF (a:\EZ_73322\single\dtmf\dtmf.exe)
This program uses the DAC section of the CODEC to output a series of Dual-Tone Multi-Frequency (DTMF) tones which are used in telephony applications. There are two possible settings for this demo

1 Generate a dial tone (the default setting) indicated by the LED on the EZKIT board being OFF

2 Generate a series of tones corresponding to a telephone number to be dialled indicated by the LED on the EZKIT board being ON.

Use the pushbutton (S1) on the AD73322 eval board to toggle between the two options. To close the demo please push the INTERRUPT button on the EZKIT board to return to the monitor program. This program processes output samples at an 8 kHz ratewhich is set by the AD73322 sample rate setting in Control Register B.

File(s) used are: \EZ_73322\single\dtmf\dtmf.dsp

Build using: \EZ_73322\single\dtmf\dtmf.bat

ADPCM (a:\EZ_73322\single\adpcm\adpcm.exe)
This program demonstrates an Adaptive Differential Pulse Code Modulation (ADPCM) algorithm providing compression to 32 kbits/sec. The AD73322 samples at an 8 kHz rate which determines the rate at which the ADPCM algorithm runs. The program allows the input/output channel to be configured for loop-through at 8 kHz or for the ADPCM algorithm to be run in a loop-through mode. The ADPCM algorithm takes the 16 bit ADC output and compresses it to an 8 bit PCM value using µ-Law coding. The 8-bit PCM value is input to the ADPCM encoder which generates a 4-bit output update value. In the loop-through, this 4-bit value is input to the ADPCM decoder whose 8-bit output is further expanded from µ-Law to 16-bit linear coding.

There are two possible settings for this demo:

1 Loop-through of input to output at 8 kHz with no compression indicated by the LED on the EZKIT board being OFF

2 Loop-through of input to output at 8 kHz featuring ADPCM indicated by the LED of the EZKIT board being ON

Use the pushbutton (S1) on the AD73322 eval board to toggle between the two options. To close the demo please push the INTERRUPT button on the EZKIT board to return to the monitor program. This program processes input and output samples at an 8 kHz rate.

File(s) used are: \EZ_73322\single\adpcm\adpcms.dsp \EZ_73322\single\adpcm\Am_thr.dsp \EZ_73322\single\adpcm\U_compre.dsp \EZ_73322\single\adpcm\U_expand.dsp

Build using: \EZ_73322\single\adpcm\adpcm.bat

AD73322 DUAL CODEC DEMO PROGRAMS

Stereo Emulation (a:\EZ_73322\dual\2in2out.exe)
This program configures a dual codec cascade to emulate a stereo codec in that one codec converts the right channel while the other codec converts the left channel. This program's code serves as a useful introduction to configuring the AD73322 for cascaded operation.

File(s) used are: \EZ_73322\dual\2in2out.dsp

Build using: \EZ_73322\dual\dual.bat

Mixed Mode Stereo Emulation (a:\EZ_73322\dual\mm_mute.exe)
This program configures a dual codec cascade, in mixed mode, to emulate a stereo codec in that one codec converts the right channel while the other codec converts the left channel. The mixed mode mode function allows the codecs to be controlled while processing ADC and DAC samples. In this demo the pushbutton switch (S1) toggles the outputs between MUTE OFF and MUTE ON. The red LED on the EZKIT LITE board is ON when MUTE is enabled.

File(s) used are: \EZ_73322\dual\mm_mute.dsp

Build using: \EZ_73322\dual\mix_mode.bat

AD73322 MULTI CODEC DEMO PROGRAMS

Three Channels (a:\EZ_73322\multi\3in3out.exe)
This program configures a three codec cascade.

File(s) used are: \EZ_73322\multi\3in3out.dsp

Build using: \EZ_73322\multi\make.bat

FourChannels (a:\EZ_73322\multi\4in4out.exe)
This program configures a four codec cascade.

File(s) used are: \EZ_73322\multi\4in4out.dsp

Build using: \EZ_73322\multi\make.bat

NOTE: New demonstration programs and revised versions of existing programs will be available for download at Analog's Website *http://www.analog.com*. Please search for the AD73322 page and choose either the *Evaluation Tools* or *Related Topics* option.

GENERAL NOTES.
The number of devices configured in cascade is programmed using the PF4 and PF5 flag I/O bits from the ADSP-2181. These bits are used to program a 74HC253 dual 4:1 multiplexer which selects the SDO/SDOFS combination from one of the four possible AD73322 codecs on the evaluation board. The settings of PF4 and PF5 for each of the possible cascade configurations is shown in the table below:

PF5	PF4	Cascade Selection
0	0	Single Codec
0	1	Two Codecs
1	0	Three Codecs
1	1	Four Codecs

Table I. Program settings for cascade configurations

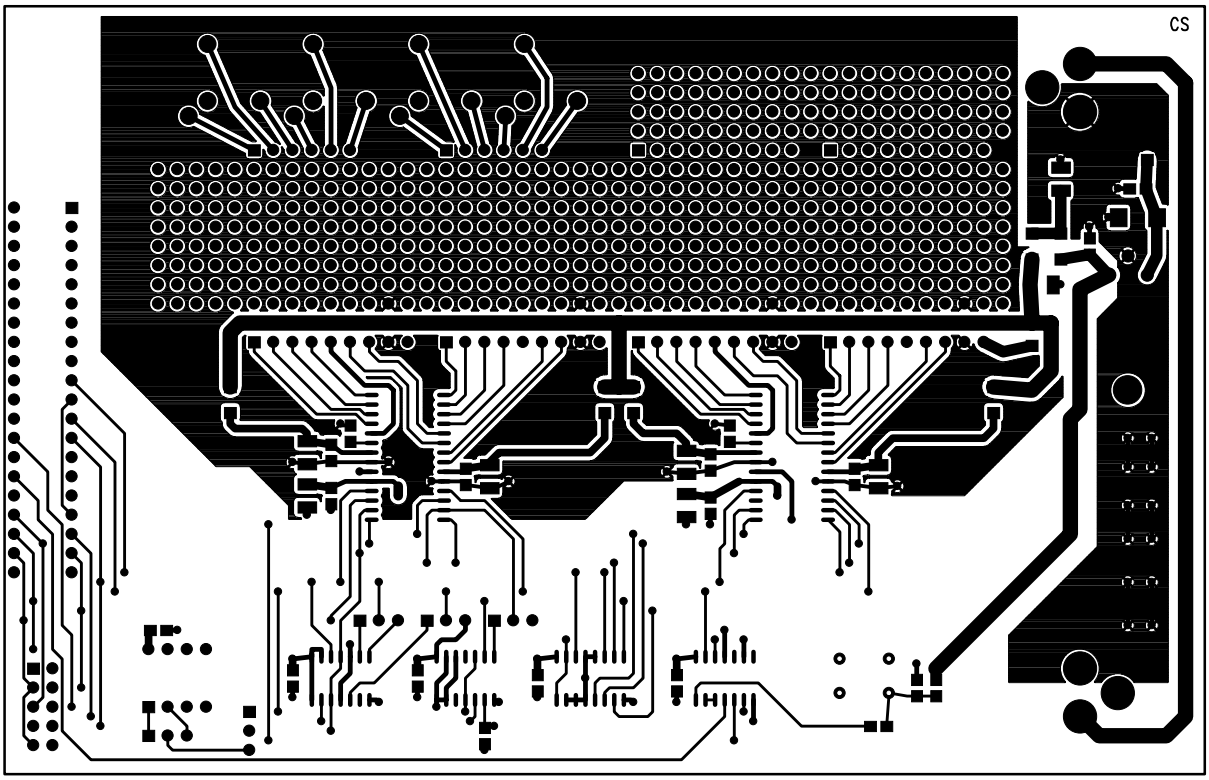

Fig. 3: EVAL-AD73322EB Main Board Component Side Artwork.

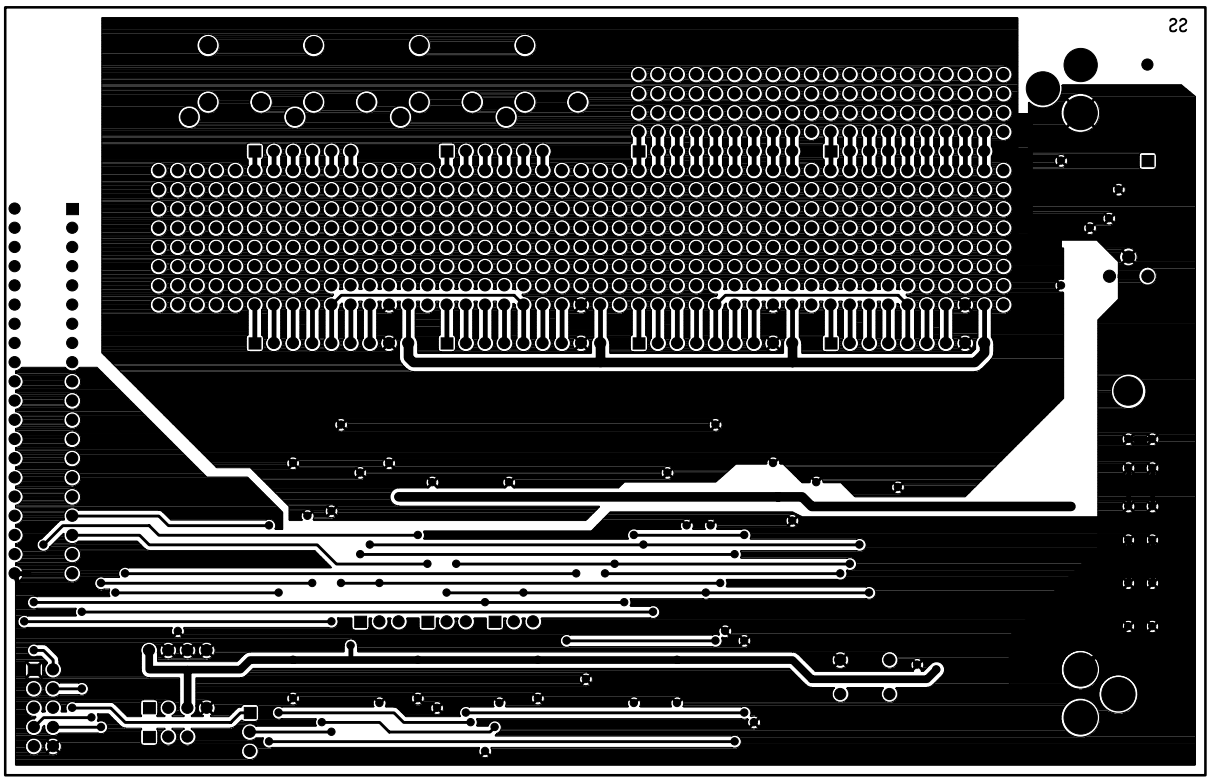

Fig. 4: EVAL-AD73322EB Main Board Solder Side Art-

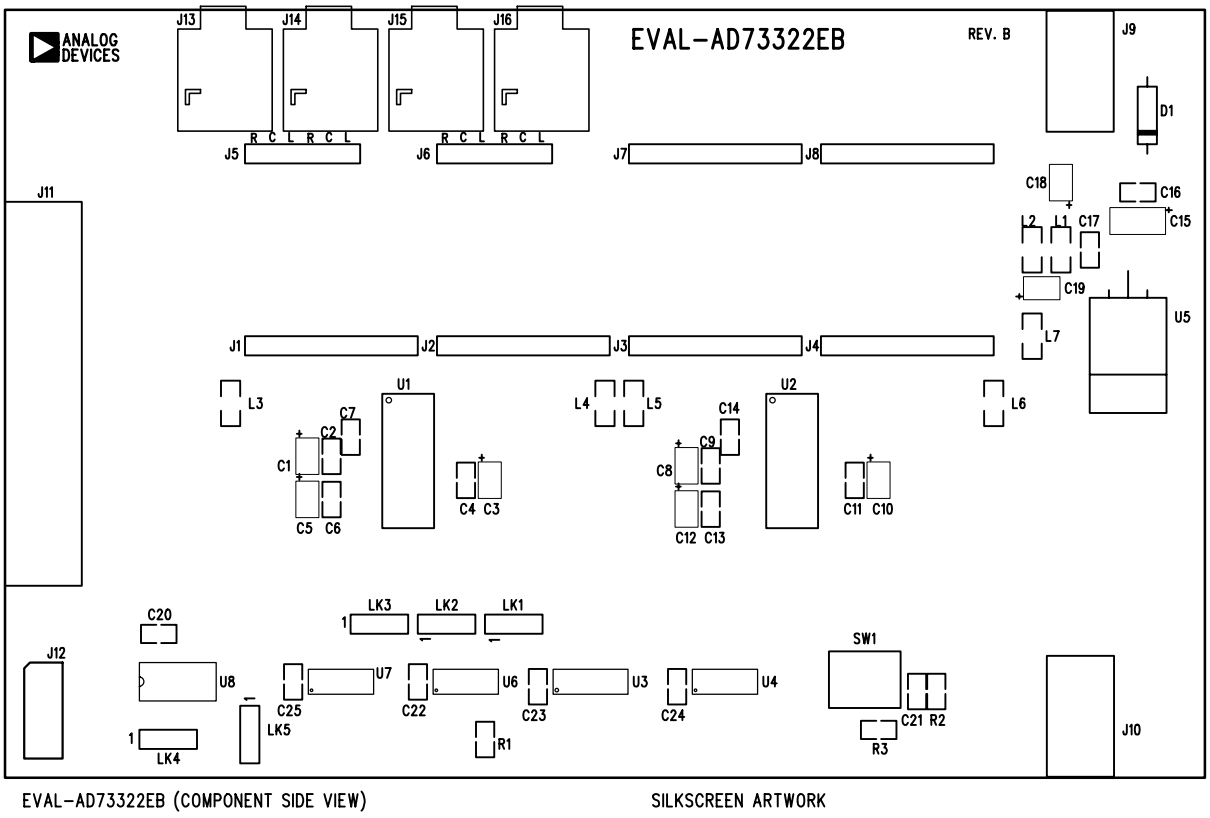

Fig. 5: EVAL-AD73322EB Main Board Silkscreen

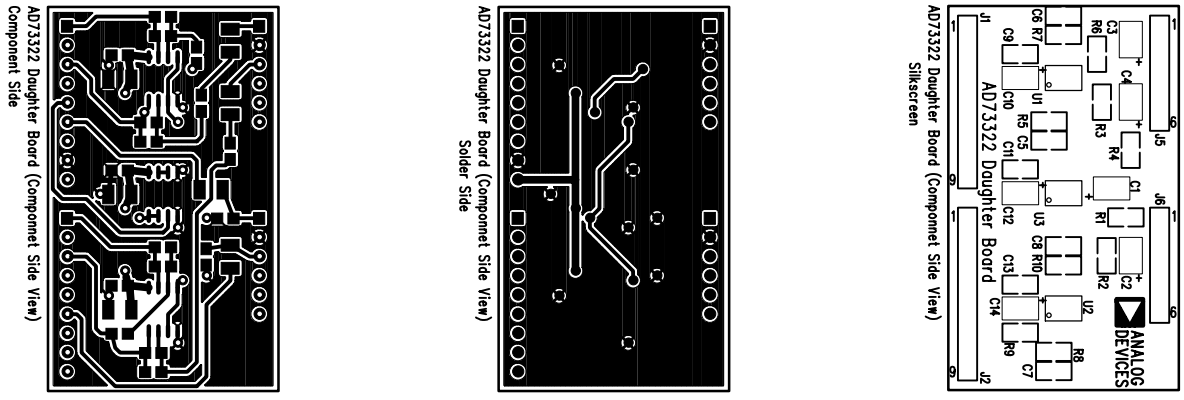

Fig. 6: EVAL-AD73322EB Daughter Board

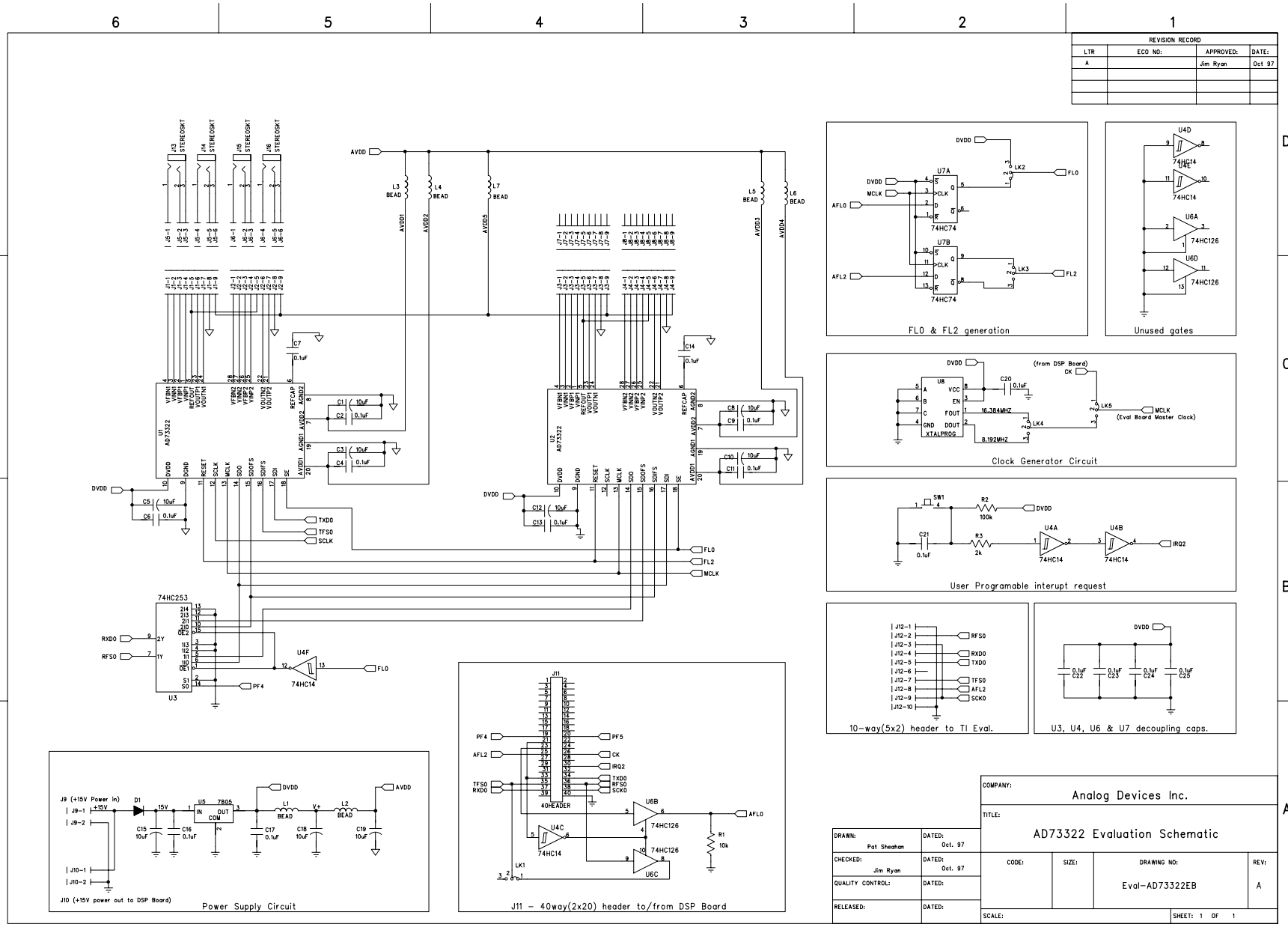

Fig. 7: EVAL-AD73322EB Main Board Schematic.

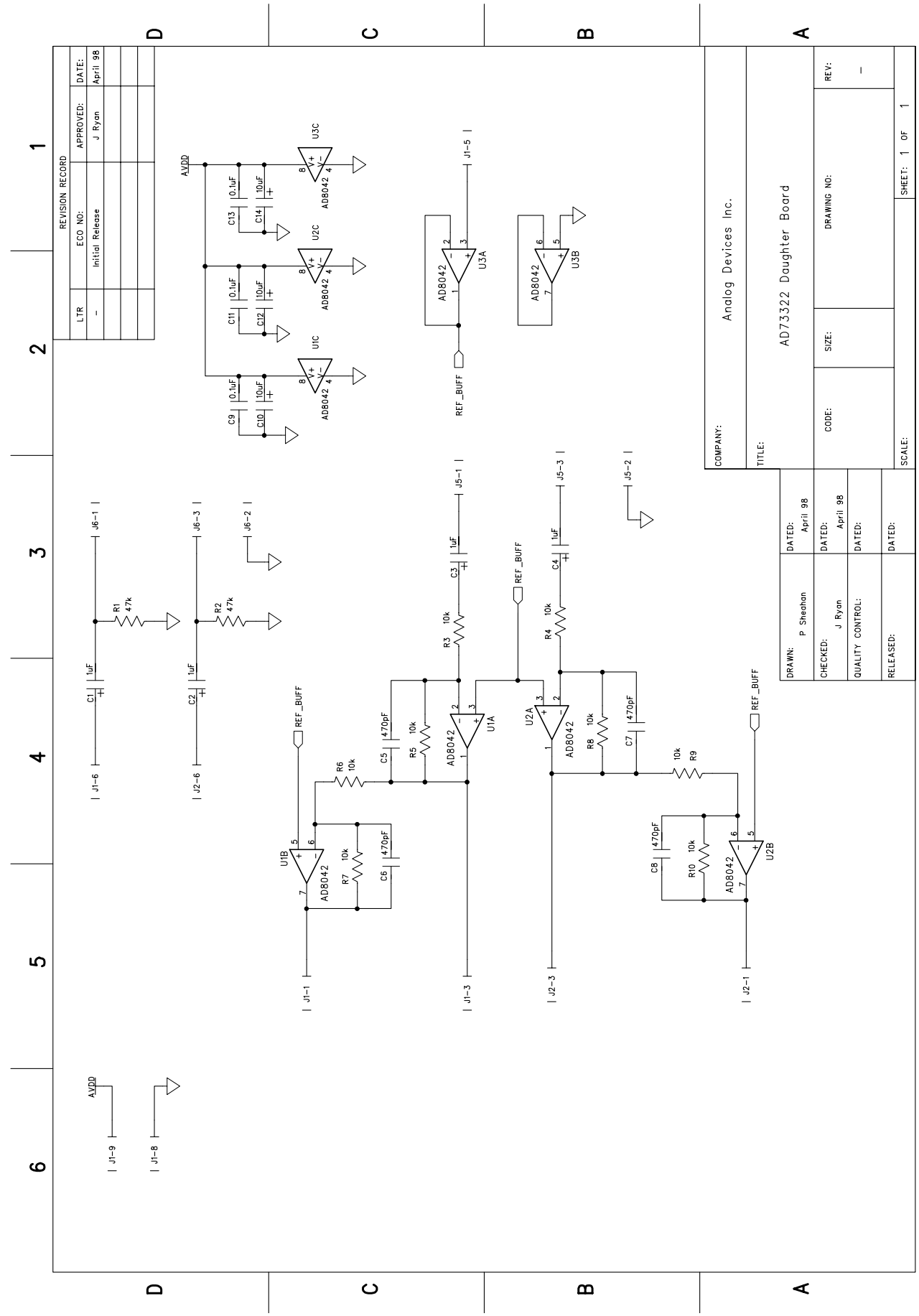

Fig. 8: EVAL-AD73322EB Daughter Board Schematic.

EVAL-AD73322EB (MAIN BOARD) BILL OF MATERIALS.

Qty	Reference Designator	Description/Value	Manuf. No.	Supplier No.
2	U1-2	AD73322	ADI AD73322AR	
1	U3	74HC253D	Motorala - MC74HC253D	
1	U4	74HC14D	Motorala - MC74HC14D	FEC 492-310
1	U5	7805CT	Motorala - MC7805CT	FEC 701-853
1	U6	74HC126D	Motorala - MC74HC126D	
1	U7	74HC74D	Motorala - MC74HC74D	FEC 492-358
1	U8	16.384MHz Prog. XTAL	Kinseki	FEC 221-740
1	D1	IN4002	Philips IN4002	FEC 365-117
9	C1 C3 C5 C8 C10 C12 C15 C18-19	10uF 16V Tant. TAJ-B Case	AVX TAJB106K016R	FEC 498-737
16	C2 C11 C6 C13-14 C7 C16-17 C4 C9 C20-25	0.1uF Ceramic 0805 Case	AVX CM21X7R104K25VAT	FEC 499-687
1	R1	10kW 5% 0.1W 0805 Case	Multicomp	FEC 613-216
1	R2	100kW 5% 0.1W 0805 Case	Multicomp	FEC 613-332
1	R3	2kW 5% 0.1W 0805 Case	Multicomp	FEC 771-375
7	L1-7	RFI Suppression Bead. 1206 Case	Steward 25Z1206-0SR	
6	J1-4 J7-8	Pin Header Socket (Top Entry) 9 way	Precidip 801-91-009-10-001	Futura
2	J5-6	Pin Header Socket (Top Entry) 6 way	Precidip 801-91-006-10-001	Futura
2	J9-10	PCB Mount Power Connector	ITT-Cannon	FEC 224-959
2	J9-10	Power Plug	ITT-Cannon	FEC 224-923
1	J11	Pin Header Socket (Side Entry) 40 way		Harwin M20-
	9884006	FEC 148-532		
1	J12	Pin Header (Dual Row) (5+5)	Harwin M20-9951006	FEC 511-808
4	J13 J14 J15 J16	3 Pole Stereo PCB Socket	Marushin	FEC 152-204
4	J13 J14 J15 J16	Stereo plug (supply loose with pcb)	Marushin	FEC 152-203
5	LK1-5	Pin Header (Single Row) (3 way)	Harwin M20-9990306	FEC 511-717
5	LK1-5	Shorting Plugs	Harwin M7567-05	FEC 528-456
1	SW1	Push Button Switch	Omron B3W1000	FEC 176-986
4	each corner	Rubber Stick-on-feet	3M SJ5076	FEC 148-922

Wire - 300mm strips - Red & Black (attach to power plugs J9 and J10, supply assembled cable with pcb)

EVAL-AD73322EB (DAUGHTER BOARD) BILL OF MATERIALS.

Intergrated Circuits

Component	Location	Vendor - Part Number
AD8042AR	U1 U2 U3	Analog Devices -AD8042AR

Capacitors

Component	Location	Vendor
1uF (TEH-X Case)	C1 C2 C3 C4	FEC - 247-583
470pF (0805 Case)	C5 C6 C7 C8	FEC - 499-195
0.1uF (0805 Case)	C9 C11 C13	FEC - 499-687
10uF 6.3V X TEH Tant.	C10 C12 C14	FEC - 286-254

Resistors

Component	Location	Vendor
47KΩ ±2% 0.1W (0805 Case)	R1 R2	FEC - 109-322
10KΩ ±2% 0.1W (0805 Case)	R3 - R10	FEC - 109-318

Connectors / Headers/Links

Component	Location	Vendor
9 Way SIL Header	J1 J2	Preci-Dip 800-10-009-10-002
6 Way SIL Header	J5 J6	Preci-Dip 800-10-006-10-002

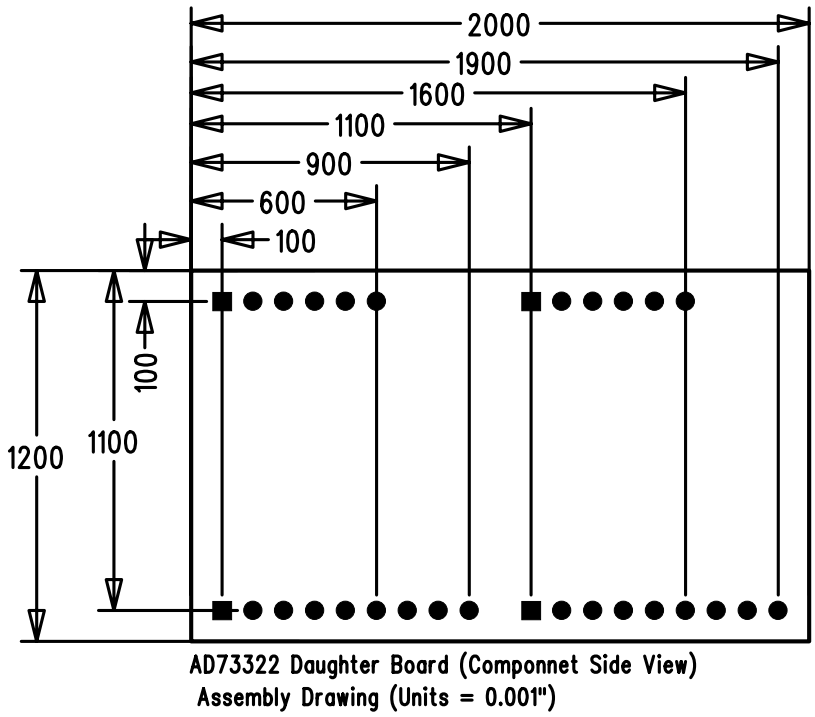

Fig. 9: EVAL-AD73322EB Daughter Board Dimensions (Not to Scale)